LOW POWER DIGITAL PULSE CONTROLLER USING FOOTER METHOD
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\textbf{Abstract:} A digitally controlled pulse width modulator (PWM) targeting on-chip power management applications is proposed in this paper. A current starved ring oscillator, with digitally controlled current source based headers and footers, is used to provide a versatile duty cycle and an accurate frequency control. The proposed circuit achieves i) a controlled duty cycle that can vary between 20\% and 90\% and ii) a compensation circuit that guarantees a constant duty cycle under process, voltage, and temperature (PVT) variations. A fast response time of 5 ns – 20ns with a fine duty cycle granularity has been achieved through the proposed control techniques. The circuit operates at a frequency range of 500 MHz – 1.66 GHz and is implemented with a 22 nm CMOS predictive technology model.

\textbf{Keywords:} Current starvation, digital-controlled oscillators, pulse width modulation, ring oscillators.

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INTRODUCTION

A pulse width modulator (PWM) is used to generate a periodic switching signal with a varying duty cycle and can be configured to control the duty of a switching signal. Various architectures have been proposed to generate pulse width modulated signals. A voltage controlled oscillator, a counter, a digital to analog converter, and a comparator are used as the building blocks of a PWM [1].

This counter based PWM requires additional clock and reference signals and therefore suffers from large power consumption. PWMs based on either a delay line multiplexor and a ring oscillator multiplexor are described, respectively, in [2] and [3] which consume less power but occupy a large chip area due to the large multiplexor circuits. PWMs based on a delay line multiplexor and a ring oscillator counter provides a means to control area/power tradeoffs [4]. A small and power efficient on-chip PWM requires a small and power efficient oscillator.

A modified ring oscillator circuit is proposed to satisfy these requirements within the PWM. Voltage controlled oscillators (VCOs) are widely used to generate a switching signal where certain characteristics of this signal can also be controlled. Two types of VCOs are primarily used in high performance integrated circuits (ICs); inductor-capacitor (LC) oscillators and ring oscillators. LC oscillators can operate at high frequencies and exhibit superior noise performance.

A conventional ring oscillator circuit is shown in Fig. 1. Duty cycle and frequency control are achieved by controlling the supply current of individual inverter stages [5]-[6]. Changing the supply current of individual inverter stages within a ring oscillator affects the transition delay characteristics of the corresponding stages, resulting in an output with a variable duty cycle. PVT variations affect the delay characteristics of the stages resulting in duty cycle variations.

Several methods have been proposed to compensate the effects of PVT variations on the performance of sensitive analog circuits. A process-invariant constant current source based on the principle of current addition has been described in [7]. Based on this principle, control
circuits can be added to provide robust duty cycle under PVT variations over a wide frequency range [5]-[6]. This principle has been used in the proposed PWM circuit. Utilizing a ring oscillator as a PVT-stable frequency source has been described in [10]-[13]. PVT compensations in these designs are either based on a band gap reference (BGR) or a sophisticated proportional to absolute temperature (PTAT) circuit that requires additional chip area. An application of PWM is shown in Fig. 2 for an inductive switching DC-DC voltage converter [8]-[9]. This circuit senses the DC-DC converter analog output (Vout) and converts this voltage to a digital signal with the analog to digital converter (ADC) block.

The digital signal is processed with control algorithm (CONTROL) that converts the signal into a pulse width modulated form. The pulse width modulated signal from (PWM) block is applied to pass transistors (M1,M2), providing a stable load current. LC filter provides a stable output voltage (Vout). The duty cycle of the generated switching signal is typically 50% for conventional ring oscillators where the PMOS and NMOS transistors within the inverters provide the same rise and fall transition times. These circuits have been typically implemented off-chip.

This work focuses on an adaptive PWM circuit that can be fully integrated on chip. The proposed PWM architecture and working principles of the ring oscillator, header, and footer control circuits are described in Section II. Simulation results and comparisons with analytic expressions are presented in Section III. Circuit comparisons and result are presented in section IV.

II. PULSE WIDTH MODULATOR ARCHITECTURE

An architectural level block diagram of the proposed PWM based on a ring oscillator is shown in Fig. 3. DC2V provides an analog control signal for the headers and footers to ensure a stable duty cycle under PVT variations. Digital control provides signals for the header and footer circuits to dynamically change the duty cycle and frequency of the ring oscillator.

A. Ring Oscillator Topology
B. PWM Control

C. Duty Cycle to Voltage Converter

D. Header and Footer Circuits.

A. Ring Oscillator Topology

A seven stage ring oscillator [5]-[6] is used for the proposed PWM as shown in Fig. 4. The odd inverter stages 1, 3, 5, and 7 are connected to header circuit Ia and footer circuit Ic. The even inverter stages 2, 4, and 6 are connected to header circuit Ib and footer circuit Id.

Conversely, an increase of the sink current through the footer Ic or Id increases the current through the NMOS devices of the inverters, enhancing the pull down capability and resulting in a faster fall time at the output. The gate voltage of these switch transistors is controlled by a digital controller to turn on and off the individual header stages. Turning on the entire header stages passes the maximum current to the ring oscillator which minimizes the duty cycle.

B. PWM Control

Analytic expressions for the duty cycle and frequency in terms of headers and footers currents from [5]-[6] and listed in the analysis in Table I are summarized here. where IA, IB, IC and ID are the currents passing through, respectively, Ia, Ib, Ic, and Id. IA5, IB5, IC5, and ID5 are the currents passing through Ia, Ib, Ic, and Id respectively, to provide a 50% duty cycle. There are primarily three different phases of this circuit. During the first phase, capacitor C1 is charged through transistor P1. In the second phase, transistors (i.e., switches) N2 and N3 are turned on to allow charge sharing between C1 and C2. At the last phase, C1 is discharged through N1.
Where $D$ is the duty cycle of proposed PWM, and $F_{\text{new}}$ is the new frequency of the PWM.

**C. Duty Cycle to Voltage Converter**

The duty cycle to voltage converter (DC2V) has been adopted from [14]. A simplified diagram of the circuit is shown in Fig. 5 and has the following cycles of operation. A high $CLK$ input charges capacitor $C_1$ from $V_{dd}$ through transistor $DM_0$.

When $CLK$ goes low, a high pulse $P_2$ turns on $DM_2$ transferring charge from capacitor $C_1$ to $C_2$. After $P_2$ goes low while $CLK$ is still low, $P_1$ goes high and discharges $C_1$ to ground through $DM_1$. The output of DC2V “$DC2V_{out}$” is used as the input “$dc2vin$” in the header and footer circuits.
III. PROPOSED FOOTER CIRCUIT

The circuit schematics for headers Ia, Ib, and footers Ic, Id are shown in Figs. 6 and 9, respectively. Addition based current sources and sinks are proposed in [6] to ensure stable and robust current delivery under PVT variations.

A modified addition based current source has been used within the header circuit using PMOS transistors PM0, PM2, PM3, and PM4. PMOS transistors PM5, PM6, and PM7 in series with PM2, PM3, and PM4 respectively control the header currents with digital inputs bx0, bx1... bxn.

A modified addition based current sink has been used within the footer circuit using NMOS transistors NM1, NM3, NM4, and NM5. NMOS transistors NM6, NM7 and NM8 in series with NM3, NM4, and NM5, respectively, control the footer currents with digital input by0, by1... byn.

Fig 6. Footer circuit Ic or Id. Digital inputs by0, by1.. byn control total footer current sinking through output port Outn.

The analog input dc2vin received from output of DC2V block provides current control for the header and footer circuits to maintain a constant current over a wide range of PVT variations.

Under PVT variations, the bias voltage for transistors PM2, PM3, and PM4 in the header circuit and transistors NM3, NM4, and NM5 in the footer circuits respectively are adjusted to maintain current values that ensure a constant duty cycle for the PWM. Device PM00 and resistor RN1 within the footer circuits provide a level shift circuit for dc2vin.

Fig. 7. Duty cycle varies between 20% and 90% with footer current IC, ID variations. Theoretical versus simulation plot.
The ratio of the header currents $IB$ to $IA$ is changed to achieve a constant frequency of 1.66 GHz, over a wide range of duty cycles. Header current ratio $IB/IA$ versus duty cycle and frequency with and without frequency compensation are shown in Fig. 8.

![Graph showing the ratio of header currents $(IB/IA)$ versus duty cycle and frequency with and without frequency compensation.]

**Fig. 8. Constant frequency simulation and theoretical comparison.**

**Table 1** Duty Cycle and frequency changes with header and footer currents

<table>
<thead>
<tr>
<th>Header or Footer Current</th>
<th>Duty Cycle</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_a$</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>$I_b$</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>$I_c$</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>$I_d$</td>
<td>↓</td>
<td>↓</td>
</tr>
</tbody>
</table>

![Footer circuit diagram showing $I_c$ or $I_d$.]

**Fig 9. Footer circuit $I_c$ or $I_d$.**

Digital inputs $by0$, $by1$, ..., $byn$ control total footer current sinking through output port Out$n$.

**IV. SIMULATION RESULTS**

The proposed PWM circuit has been implemented with 22 nm CMOS predictive technology model. Simulation results of the PWM are compared with expressions defined in Section II.
Fig. 10. combined heater and footer circuit

Fig. 10.1 combined heater and footer output waveform

Fig. 10. 2 power calculation table in header and footer circuit
A comparison of the proposed PWM with state-of-the-art PWMs is provided in Table III. The proposed PWM can be implemented in a small area and consumes significantly less power over a wide frequency range.

Table III - Area, Power and Frequency of Operation Compared

<table>
<thead>
<tr>
<th>Design</th>
<th>Area (mm²)</th>
<th>Power/Frequency</th>
<th>Technology (CMOS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>0.55</td>
<td>10.5 mW/300 kHz</td>
<td>0.60 nm</td>
</tr>
<tr>
<td>[9]</td>
<td>1.00</td>
<td>11.2 mW/1.25 GHz</td>
<td>0.13 um</td>
</tr>
<tr>
<td>[10]</td>
<td>1.20</td>
<td>19.2 mW/2.4 GHz</td>
<td>0.25 um</td>
</tr>
<tr>
<td>[11]</td>
<td>3.20</td>
<td>1.0 mW/200 kHz</td>
<td>0.35 nm</td>
</tr>
<tr>
<td>[12]</td>
<td>2.00</td>
<td>0.15 mW/278 MHz</td>
<td>65 nm</td>
</tr>
<tr>
<td>This work</td>
<td>0.6</td>
<td>0.2 mW/1.66 GHz</td>
<td>16 nm (DC)</td>
</tr>
</tbody>
</table>

*Estimated area= device area x 5, power=simulation estimate.*

V. CONCLUSIONS

A digitally controlled PWM has been proposed that adaptively changes the header and footer current profiles to maintain a constant duty cycle under PVT variations. The proposed circuit can adaptively control the duty cycle and the frequency at runtime. A DC2V converter and novel header and footer circuits are employed to achieve a stable duty cycle operation under PVT variation.

REFERENCES


