AUTOMATIC TEST PATTERN GENERATION TECHNIQUE FOR TESTING COMBINATIONAL CIRCUITS

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Abstract: An Automatic test pattern generation technique using a pseudo-random number generator algorithm for testing combinational circuit is proposed. Rather than targeting a single fault pair at a time, the proposed System approach can distinguish multiple fault pairs in a single instance. For generation of automatic multiple non-repeating inputs which is used for testing the combinational circuit. Pseudo-random generator can be used. New approaches are needed to reduce execution time and to improve fault coverage. We compare lehmer linear congruential algorithm with Galois-LFSR with respect to Area, Time performance and power dissipation.

Keywords: Pseudo-random number generator; ATPG; Algorithm; Testing; Fault distinguishing

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INTRODUCTION

A common objective of testing is to detect all or most modeled faults. Although fault coverage has a somewhat nonlinear relationship with the tested product quality or defect level (parts per million), for practical reasons fault coverage continues to be a measure of the test quality. The increase in the design complexity and reduced feature sizes has elevated the probability of manufacturing defects in the silicon. These defects could result from shorts between wires/vias, breakage in wires/vias, transistor opens/shorts, etc. Fault diagnosis is the process of finding the fault candidates from the erroneous response. Any vector that can produce different responses for two different faults is called a distinguishing vector for those faults. Hence, to reduce the number of fault candidates, a test set that is able to distinguish between all distinguishable faults is highly desirable. The process of generating such distinguishing patterns is termed as Diagnostic Pattern Generation. The goal of an automatic diagnostic pattern generation (ADPG) is to generate a set of test patterns that is able to both detect all the detectable faults and make fully distinguishable all (detectable) faults that are not equivalent to each other. In general, we often prefer such a set of vectors to contain a small number of vectors. Most test generation systems are built around core ATPG algorithm for

(1) Finding a test vector for a target fault

(2) Simulating faults to find how many have been detected by a given vector. The system then attempts to find tests of high fault coverage because the primary objective is fault detection, i.e., presence or absence of faults. Basically, we generate tests that are redundant for fault detection and then hope that they will provide better diagnostic capability. To reduce the excess tests we may resort to optimization or removal of unnecessary tests. Conventional ADPG engines target single fault pairs at a time with Boolean values only. However, targeting single fault pairs may miss opportunities to find vectors that can simultaneously distinguish multiple pairs.

New approach include diagnostic test generation technique using a pseudo-random generator algorithm that can produce a compact diagnostic test set that can distinguish all the distinguishable fault pairs. Such a formulation allows for efficient handling of multiple fault pairs, and each diagnostic test vector generated will be able to distinguish a large number of fault pairs at each iteration. Subsequently, smaller diagnostic test sets are generated. Deterministic test pattern generation algorithms are highly complex and time-consuming. New approaches are needed to reduce execution time and to improve fault coverage. An approach which provides the testing of the combinational circuit by providing multiple non-repeating test
inputs in the text file format and the response of the circuit to those inputs will be available in
the text file format. Comparison of the generated outputs with the standard required outputs
leads to the fault identification in the combinational circuit.

II. PSEUDO-RANDOM NUMBER GENERATOR

A pseudorandom number generator (PRNG), also known as a deterministic random bit
generator (DRBG) is an algorithm for generating a sequence of numbers that approximates the
properties of random numbers. The sequence is not truly random in that it is completely
determined by a relatively small set of initial values, called the PRNG's state, which includes a
truly random seed. Although sequences that are closer to truly random can be generated using
hardware random number generators, pseudorandom numbers are important in practice for
their speed in number generation and their reproducibility.

We use linear congruential method for generating random numbers which was introduced by
D.H. Lehmer in 1949 which uses recurrence to generate numbers i.e.

\[ S_i = (a \times S_{i-1} + c) \mod m \] ------ (1)

Where, m = modulus

a = positive integer called the multiplier and

c = positive integer called the increment

The Linear Congruential method has the advantage of being very fast, requiring only a few
operations per call, hence it is almost used universally. The above recurrence (1) will eventually
repeat itself, with a period that is obviously no greater than m. If m, a, and c are properly
chosen, then the period will be of maximal length, i.e. of length m.

III. AUTOMATIC TEST PATTERN GENERATION METHODS

The classical ATPG methods target the problem at the logic level and might require large
amounts of computing time and resources to generate tests for even moderately sized
sequential circuits [1]. In order to reduce the complexity of sequential ATPG, various design for
testability (DFT) schemes have been proposed that alter the circuit structure and functionality
in the test mode to make the circuit easily testable.

The different diagnostics test generation methods are as follows:
A. Diagnostic test generation Method:

Diagnosis plays a crucial role in cutting down testing cost and improving yield. In 1982, J. Savir and J. P. Roth proposed the Diagnostic test generation was first introduced using a D algorithm in Testing for and distinguishing between failure. Later instead of exclusively finding test patterns that can distinguish all fault pairs in the circuit, finding distinguishing patterns only those faults not yet distinguish by the ATPG.

B. Modification in ATPG System:

A method of modifying ATPG tool to generate diagnostic patterns in A Fast Diagnostic Test Pattern Generator for Combinational Circuits was proposed by T. Gruning, U. Mahlstedt and H. Koopmeiners in Nov. 1991. In the year 2003, V. Agrawal, D. H. Baik, Y. C. Kim, and K. Saluja proposed an exclusive test for a pair of faults as a test that detects exactly one fault from a given pair of a fault in Exclusive Test and its Applications to Fault Diagnosis. M. Chandrasekar, N. P. Rahagude, and M. S. Hsiao proposed an incremental learning-based ADPG flow was proposed which incrementally utilized the information learned during ATPG for ADPG in Search State Compatibility Based Incremental Learning Framework and Output Deviation Based X-filling for Diagnostic Test Generation in the year 2010.

After that I. Pomeranz and S. Reddy proposed an output dependent approach for diagnostic test generation was proposed in which outputs of the circuit are considered one at a time in Output-Dependent Diagnostic Test Generation.

C. SMT-based Diagnostic Test Generation Method:

In the year 2012, Sarvesh Prabh, Michael S. Hsiao, Loganathan, Lingappan and Vijay Gangaram proposed a new diagnostic test generation technique using a SMT formulation that can produce a compact diagnostic test set that can distinguish all the distinguishable fault pairs in A SMT-based Diagnostic Test Generation Method For Combinational Circuits. The problem of evaluating the satisfiability of first order formulas with respect to some background theories is called Satisfiability Modulo Theory (SMT) [1].

When solving an instance, each atom in the SMT formula is internally assigned a Boolean variable. The Boolean formula is solved by an underlying SAT solver. such a formulation allows for efficient handling of multiple fault pairs, and each diagnostic test vector generated will be able to distinguish a large number of fault pairs at each iteration. Subsequently, smaller diagnostic test sets are generated.
D. A Text I/O File based ATPG Technique:

Conventional ADPG engines target single fault pairs at a time with Boolean values only. However, targeting single fault pairs may miss opportunities to find vectors that can simultaneously distinguish multiple pairs. Our approach will be to increase the quality of generated IC using VLSI design, by efficiently generating all the possible tests for determination of output. Generation of all the possible input pairs of testing will lead to the use of Random Number Generator. Earlier methods used conventional method using keypad which takes human efforts to manually enter the input combinations. The ability of random number generators to generate all the possible pairs of inputs will be utilized to generate inputs. Corresponding outputs will be noted. The noted outputs will be compared with the actual expected outputs for given input combination.

An approach is a new diagnostic test generation technique using Pseudo-random number generator which is the algorithm that can automatically produce long runs of number with good random properties that can produce a compact diagnostic test set that can distinguish all the fault pairs. For generation of automatic multiple non repeating inputs which are used for testing the combinational circuits, pseudo-random generator can be used. Such a formulation allows for efficient handling of multiple fault pairs, and each diagnostic test vector generated will be able to distinguish a large number of fault pairs at each iteration. The VLSI combinational circuit is developed by writing it in either the VHDL language. The program so written is checked for errors, if any, in the Quartus II 9.1 SP2. The RTL view of the VLSI combinational circuit may also be seen.

Fig.1 Line of action
IV. CONCLUSION

The proposed a Text based Automatic test pattern generation technique for testing the combinational circuits using pseudo-random generator algorithm that can target multiple fault pairs rather than targeting a single fault pair in single iteration. It requires less power consumption and improve testing efficiency.

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REFERENCES


